Claim 18. (currently amended) A method for automatically producing clock signals for sampling data signals at different data rates via the phase locked loop as claimed in claim 16, the method further comprising the step of:

processing, once the protocol identification information has been ~~detected~~identified, at least some of respective overhead information.

Claim 19. (currently amended) An apparatus for automatically producing clock signals for sampling data signals, which are transmitted with the aid of transmission protocols, at different data rates, the data signals having at least one binary protocol identification information item which uniquely identifies ~~the~~ a transmission protocol, the apparatus comprising:

a phase locked loop for synchronization of a clock signal to a ~~digital~~ data signal passed to a phase/frequency control device;

at least one controllable frequency divider device arranged in a feedback path of the phase/frequency control device;

~~a sampling device for sampling the data signal with the aid of the clock signal;~~

a control unit for ~~setting~~ selecting and varying the clock signal to ~~a frequency which corresponds to a transmission protocol~~ frequencies corresponding to different respective transmission protocols; ~~and~~

a sampling device for sampling, during a synchronization process, the data signal successively using the clock signal at different frequencies which are associated with different transmission protocols, using varied clock signals set by the control unit; and

a protocol detector in which the control unit is arranged, the protocol detector storing at least a portion of the sampled data signal and ~~investigating~~ checking the ~~sample~~ sampled data signal during the synchronization process for the presence of protocol identification information associated with a selected clock signal until the protocol identification information of ~~a~~ the transmission protocol is identified~~and transmitting an investigation result to the control unit which, if there is no protocol identification information, selects further defined frequencies for the clock signal until the protocol identification information is identified in the sampled data signal~~.

Claim 20. (currently amended) An apparatus for automatically producing clock signals for sampling data signals as claimed in claim 19, further comprising:

a memory connected to the control unit, the memory being arranged in the protocol detector for storing the at least one binary protocol identification information item and at least one control device control information item associated with the respective binary protocol identification information item, which controls ~~and controlling~~ the phase locked loop on a protocol-specific basis, wherein the control unit forms at least one control signal from the at least one control device control information item, with the at least one control signal being transmitted to the phase locked loop, wherein; ~~and~~

~~a detector connected to the control unit and arranged in~~ the protocol detector ~~for detecting the stored protocol identification information which is associated with the at least one control device control information item in the sampled data signal, wherein the detector~~ produces a control signal representing ~~a detection~~an identification result which is transmitted to the control unit, and wherein the control unit is designed such that at least one control signal, representing a frequency divider control information item, is formed from the at least one stored control device control information item and is transmitted to the at least one controllable frequency divider device.

Claim 21. (currently amended) An apparatus for automatically producing clock signals for sampling data signals as claimed in claim 20, wherein the control unit is designed such that, if a ~~number~~plurality of protocol identification information items are stored in the memory, ~~the~~ control device control information items associated with the ~~number~~ plurality of protocol ~~binary~~ identification information items are transmitted successively to the phase locked loop, and the respectively associated binary protocol identification information items are detected successively ~~in the sampled data stream~~, with the control device control information items being transmitted successively as a function of the ~~detection~~ identification result.

Claim 22. (currently amended) An apparatus for automatically producing clock signals for sampling data signals as claimed in claim 20, wherein the protocol detector comprises:

a shift register to which the ~~sample~~ data signal or the sampled data signal, ~~the data signal~~ and the clock signal are passed;

a comparator connected to both the shift register and the control unit; and

a memory register connected to both the comparator and the control unit for temporary storage of the protocol identification information;

wherein the comparator is designed such that the protocol identification information stored in the memory register is compared with the data signal or the sampled data signal read to the shift register and a comparison result is transmitted to the control unit with the aid of the control signal.

Claim 23. (currently amended) An apparatus for automatically producing clock signals for sampling data signals as claimed in claim 20, wherein different protocol identification information items and overhead control information items associated therewith are stored in the memory, the ~~sample~~ sampled data signal is supplied to ~~an overhead processing unit which is connected to~~ the control unit for processing protocol-specific overhead information included in the data signal, and the overhead processing unit and the control unit are designed such that the overhead information is processed as a function of ~~the~~ at least one overhead control information item associated with the ~~detected~~ identified transmission protocol.

Claim 24. (previously presented) An apparatus for automatically producing clock signals for sampling data signals as claimed in claim 20, further comprising:

a control/monitoring interface to which the control unit is connected, via which information stored in the memory can be updated and detection results can be transmitted to a higher-level communications unit.

Claim 25. (currently amended) An apparatus for automatically producing clock signals for sampling data signals as claimed in claim 20, wherein a number of voltage controlled oscillators provided in the phase-locked loop can be selected as a function of the at least one control device control information item.

Claim 26. (previously presented) An apparatus for automatically producing clock signals for sampling data signals as claimed in claim 20, further comprising:

a frequency window discriminator provided in the phase locked loop which defines a frequency of the clock signal as a function of the at least one control device control information item and is set by the control unit.

Claim 27. (currently amended) An apparatus for automatically producing clock signals for sampling data signals as claimed in claim 19, further comprising:

a loop filter provided in the phase locked loop ~~which is set by the control unit~~.

Claim 28. (currently amended) A method for automatically producing clock signals for sampling data signals as claimed in claim 15, wherein the transmission protocol is selected from the group consisting of Synchronous Transport ~~Module~~ modules 1, 4 and ~~6~~ 16 (STM-1, STM-4, STM-16), fiber channel and Gigabit-Ethernet protocols.